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System Development and Programming with the 3rd and 4th Generation SHARC Processors

Course Name:	System Development and Programming with the 3rd and 4th Generation SHARC Processors
Course Code:	WS_SHDEV
Course Description:	This is a practical course with 'hands on' training using the latest VisualDSP++ software development tools. The course starts with getting a good working understanding of the VDSP++ development environment, including the development of a simple 'C' application. Next, the core elements of the SHARC, which includes the Computational Units, the Data Address Generators, and the Program Sequencer, are examined in detail along with a brief overview of the relevant assembly code instructions. The core section is common to all members of the SHARC family. A number of simulator labs help in understanding operation of the individual elements. Memory configuration (both internal and external) is discussed next. Advanced instructions and SIMD operation are presented with a follow on lab on code optimization. The I/O peripherals, which include the DAI and DPI, are discussed in detail along with DMA operation between these peripherals and internal memory. This section also deals with system booting. Hardware development tools, such as evaluation boards and ICE's are introduced with a follow on instructor led demonstration of an interrupt driven application for a hardware target. Throughout the course, the various aspects of the software development process using the latest tools are discussed including setting up and building projects, 'C' and assembly language programming, code debugging, simulation, and VDK.
Goals and Objectives:	The main course objective is to understand the SHARC architecture (with a focus on the ADSP-2136x/37x/4xx Sharc Processor Family members) sufficiently to enable DSP system designers to resolve hardware/software issues with their applications. Additional goals include gaining a thorough understanding of SHARC code development (using both assembly and 'C') using the latest software tools.
Pre-requisites:	Previous embedded microprocessor experience (hardware and/or software) would be an asset.
Target Audience:	System Designers needing to make informed decisions on design tradeoffs, Hardware Designers needing to develop external interfaces and low level code, and Code Developers needing to know how to get the highest performance from their algorithms
Duration:	3.5 days